Design and characterization of silicon carbide photoconductive switches for high field applications

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Characteristics of a silicon carbide photoconductive switch designed for high field applications have been studied. Analyses show that premature breakdown occurs primarily due to impact ionization and subsequent charge accumulation near the anode. For the shallow donor, deep-acceptor-type compensated material, a p^+ layer next to the cathode results in field homogenization in the bulk. As a result, the blocking or hold off voltage of the switch could increase beyond the experimentally determined value of 18 kV (0.45 MV/cm). Simulations also show that a minimum thickness, equivalent to a diffusion length, of the p^+ layer is necessary to avoid premature breakdown. Following illumination, the photocurrent rise time of the switch would also improve by about 25% with the p^+ layer near the cathode. © *2006 American Institute of Physics*.
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I. INTRODUCTION

An important application of a photoconductive semiconductor switch (PCSS) is in circuits for generating pulsed power.[1,2] Such configurations require minimum off-state leakage current and minimum pulse rise time.[3] Switch stability, specifically breakdown at high fields, and useable lifetime following a number of switching operations is still a concern. Both Si and semi-insulating GaAs PCSS have been used in many high power applications. However, semi-insulating SiC is also a viable candidate because of its stable characteristics at high temperature, high band gap, and large electron saturation velocity.[4,5] SiC PCSSs also offer other advantages, both at low field and in high voltage pulse formation configuration. Recently, a number of studies have been devoted to the analysis of SiC PCSS.[6,7]

GaAs has been employed as a linear photoswitch material due to its high electron mobility and large dark resistivity. The large mobility reduces the optical energy requirements necessary to produce a given conduction resistance. SiC on the other hand has comparatively much lower electron mobility but yet can be designed for linear mode operations without an increase in optical closure energy. This is possible because of the material characteristics itself. A very low mobility in SiC is more than compensated by the very high breakdown strength (3×10^6 V/cm) and, as discussed below, makes it a viable alternate material for linear mode operations[6]

$$R_{C\text{-GaAs}} = \frac{E_\lambda h_{s\text{-GaAs}}^2}{\mu_{e\text{-GaAs}} q_e E_{o\text{-GaAs}}}. \tag{1}$$

Equation (1) is an expression for the conduction resistance of a GaAs PCSS, where E_λ is the energy of the incident photon in eV, h_s represents the switch height (distance between the contacts, see Fig 1) in centimeter, μ_e is the electron mobility, q is an electron charge (1.6×10^{-9} C), and E_0 is the incident optical energy in joules.[1] The suffix GaAs represents gallium arsenide.

One can write a similar expression for SiC and after dividing one by the other and further mathematical manipulations one can write.[7]

$$\frac{E_{o\text{-SC}}}{E_{o\text{-GA}}} = \left(\frac{h_{s\text{-SC}}}{h_{s\text{-GA}}}\right)^2 \left(\frac{\mu_{e\text{-GA}}}{\mu_{e\text{-SC}}}\right) = \left(\frac{E_{B\text{-GA}}}{E_{B\text{-SC}}}\right)^2 \left(\frac{\mu_{e\text{-GA}}}{\mu_{e\text{-SC}}}\right) \approx 0.16. \tag{2}$$

Equation (2) gives the ratio of optical control energies that result in the same conduction resistance using the same photon energy in both the cases. Since the mobility in GaAs is six times that of SiC, the right hand mobility terms enhance the ratio in Eq. (2); however, the operating electric field of SiC PCSS is much greater than that of GaAs (12 times higher). By assuming the E field to be only six times higher, one can show that the thickness of the SiC will be 1/6th of that of GaAs. If the band gap or sub-band-gap radiation is used to illuminate the respective materials only 34% of the optical energy is necessary to produce the same conduction resistance in SiC as compared to a GaAs switch. Thus the linear SiC switch can be used at much lower optical power; a remarkable improvement in the specification of linear PCSS. Operations in the linear mode, together with bias enhancement mechanism suggested in this paper, could help in

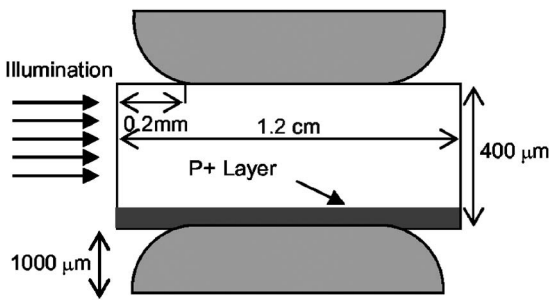

FIG. 1. UMC SDDA 6*H* SiC high power compact switch geometry.

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operating the SiC PCSS at a higher breakdown voltage than is current possible.

This paper is a follow-up of our previous study where we have analyzed the material characteristics and the early breakdown mechanisms of a compact SiC PCSS at low fields.[8] In this paper we identify the mechanism for early breakdown and propose design criteria for high bias operation. We then analyze a switch design for high field and study its characteristics, specifically the relationship between the material compensation mechanism and its effect on high field operation. The paper is organized as follows. In Sec. II, we briefly describe the switch fabrication, illumination characteristic, and simulation at low power, while in Sec. III a mechanism to improve the device operation at high power is presented. We present our conclusion in Sec. IV.

II. LOW FIELD ILLUMINATION AND SIMULATION MATCH

High resistivity 6*H* SiC can be either intrinsic or compensated. Most PCSS applications use compensated materials involving deep/shallow donors and acceptors.[9–11] Vanadium in 6*H*-SiC, is an amphoteric, deep impurity level, and is used with either a shallow acceptor (boron) or a shallow donor (nitrogen) in the compensation scheme. For vanadium-boron compensation, the material is the deep donor shallow acceptor (DDSA) type while nitrogen compensation makes it the shallow donor deep acceptor (SDDA) material. The PCSS used in this analysis is a SDDA material with a deep vanadium acceptor trap concentration of $2\times10^{16}/\mathrm{cm}^3$ and a shallow nitrogen concentration of $2\times10^{15}/\mathrm{cm}^3$.[8]

The switches studied in this analysis were fabricated at the Lawrence Livermore National Laboratory (LLNL). A square, *a*-plane rather than the *c*-plane slab ($1.2\times1.2\times0.04\ \mathrm{cm}^3$) was used to avoid micropipes problem.[12] Both the surfaces were polished before a 200 nm nickel layer was annealed at 1273 K for 2 min to form a uniform NiSi layer. A 100 nm titanium layer was then added, followed by a 100 nm platinum, and 500 nm of gold deposition. Indium solder was then used to bond the gold layer to copper electrodes. The radius of the copper electrode is 0.2 cm (Fig. 1), and the electrode separates from the surface of the SiC slab at around 0.4 cm from the center of the switch. Further details are provided elsewhere.[8]

The test setup for photoconductivity has three major components, which includes the pulse power system, the photonic system, and the measurement system (Fig. 2). The pulse power system is a regulated dc voltage supply that charges a 1.4 nF capacitor. This capacitor is then discharged into a 14 m coaxial transmission line via an optically triggered insulated gate bipolar transistor (IGBT) circuit. When the IGBT switch is closed, the resulting current resonantly charges the transmission line section to apply voltage to the SiC switch residing in the test bed. When the voltage across the SiC switch is maximum, a 532 nm laser pulse generated by the photonic system is injected into the edge of the SiC slab. The photonic system is composed of a Continuum Surelite II Nd:YAG (yttrium aluminum garnet) laser to deliver a 10 ns, 532 nm laser pulse into the SiC switch at the precise

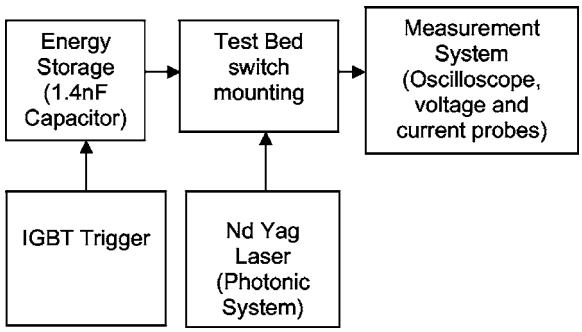

FIG. 2. Schematics of switch pulse charging setup.

time that the voltage pulse arrives. The third system is the measurement system. It consists of a set of electrodes that form the test bed, a Tektronix high voltage (HV) probe, a T&M Research Products shunt current probe, and a Tektronix dp8446, digital phosphorous oscilloscope. In the test a 1 cm diameter laser beam was focused with a cylindrical lens and used to illuminate the edge of the SiC in the switch. The 532 nm, 10 ns laser pulse was applied at the peak of the 340 V, 3 μs voltage pulse [Fig. 3(a)]. A peak photocurrent of 6 A was obtained through a load resistance of 53 Ω (on state switch resistance of ~3 Ω) [Fig. 3(b)].

The PCSS simulation scheme consists of numerical solutions to the drift, diffusion, generation, recombination, and the continuity equations. In addition, the trap levels in the compensated material are accounted for in Poisson's equa-

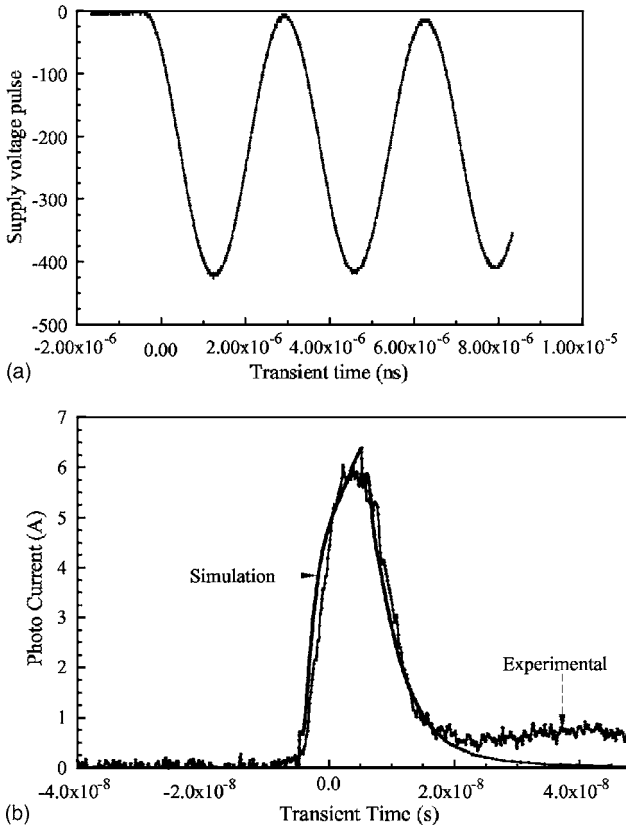

FIG. 3. (a) Supply voltage pulse with open load and (b) simulation and experimental photocurrent characteristics at low bias (switch it triggered at the peak of input voltage pulse).

tion and in the trap assisted tunneling model, etc.[13] The trap occupancy factor is incorporated through Eq. (1)–(4),

$$F_n = \frac{\upsilon_n \sigma_n + e_p}{\upsilon_n(\sigma_n + \sigma_p) + (e_n + e_p)}, \tag{3}$$

$$F_p = \frac{\upsilon_p \sigma_p + e_n}{\upsilon_n(\sigma_n + \sigma_p) + (e_n + e_p)}, \tag{4}$$

$$e_n = g_0 \upsilon_n \sigma_n n_i \exp \frac{E_{\text{level}} - E_i}{kT_L}, \tag{5}$$

$$e_p = \frac{1}{g_0} \upsilon_p \sigma_p n_i \exp \frac{E_i - E_{\text{level}}}{kT_L}, \tag{6}$$

where υ_n and υ_p are thermal velocities for electrons are holes, respectively, σ_n and σ_p are capture cross sections, e_n and e_p are emission rates, n and p represent electron and hole densities, respectively, and n_i is the intrinsic carrier concentration. Also, E_i is the intrinsic fermi level position, E_{level} is the energy level of each discrete trap level in the band gap, g_0 is the degeneracy factor of the trap center, k is Boltzmann's constant, and T_L is the lattice temperature. Also, the trap generation and recombination terms were included by the following equation:[14]

$$R = \sum_{\alpha=1}^{k} R_n^{\alpha} + \sum_{\beta=1}^{m} R_p^{\beta}, \tag{7}$$

where k is the number of donorlike traps, m is the number of acceptorlike traps, and $R_{n,p}$ can be written as[13]

$$R_{n,p} = \frac{pn - n_i^2}{\tau_n\{p + (q/g_0)n_i \exp[(E_i - E)/\ kT_L)]\} + \tau_p\{n + g_0 n_i \exp[(E - E_i)/kT_L]\}}. \tag{8}$$

Consequently, the electron and hole lifetimes are trap dependent shown as

$$\tau = \frac{1}{\sigma \upsilon N_T}, \tag{9}$$

where N_T is the discrete trap density/cm^3. The Auger recombination model is also included in the simulations. For laser illumination, an optical efficiency of 100% was assumed and the optical absorption coefficient used was 0.5 cm^{-1}.[15] Also, since material in intimate contact with SiC is expected to affect the injection behavior prominently, only nickel silicide is used as contact material for the simulations. The actual contact has three layers of metals, as discussed earlier.

The experimental and simulated illumination results (Fig. 3) were in good agreement at the optical power absorbed at 532 nm wavelength, which was around ~7 kW/cm^2. A good match at low power validated the model parameters used in this study and also provided useful insights into the workings of the PCSS during a switching, which was the basis for design changes for high power operations. A comparison with experimental values also indicated that only 5%–7% of the optical energy was actually absorbed in the device. This could be attributed primarily to reflections (the surface of the SiC slab need machining), as well as to low optical and quantum efficiencies, etc.[16] Improving low optical absorption (e.g., by polishing of surfaces) is a part of our research effort at UMC. Also, the use of antireflection coating to improve the absorption will be considered in the next batch of switches.

III. HIGH FIELD OPERATION ANALYSIS

The electric field distribution in a PCSS greatly influences the device operation and the two important switch parameters such as voltage standoff and rise time. Hence the field profile in the bulk is a good measure of the switch performance. The material hold off characteristic is influenced by the semi-insulating conductivity of the bulk rather than space-charge depletion, as is the case with a *pn* junction.[7] For the SiC PCSS under consideration, the bulk electric field decreases from the anode to the cathode, as in Eq. (9), which is based on a solution to Poisson's equation (8), incorporating trap densities,[17]

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_0 \varepsilon_s}[n(x) - N_{\text{di}}^{+}(x) + N_{\text{ai}}^{-}(x)] \tag{10}$$

where $n(x)$ is the electron concentration, N_{di}^{+} is the ionized donor concentration, N_{ai}^{-} is the ionized compensating acceptor concentration, and $N_{d,\text{si,eff}} = N_d$. Solution for the E field gives

$$E_x(x) = \frac{qN_{d,\text{si,eff}}}{\varepsilon}(l - x), \tag{11}$$

where l is the length of the switch and x is the distance variable.

The high fields contribute to impact ionization, thus causing a large number of secondary electrons to reach the anode without being collected. The electric fields thus terminate at the "virtual cathode" very near the anode. The enhanced field results in contact degradation and premature breakdown at 18 kV (450 kV/cm), which has been experimentally observed earlier.[8] The breakdown mechanism is similar to the gate rupture or burnout of metal-oxide-

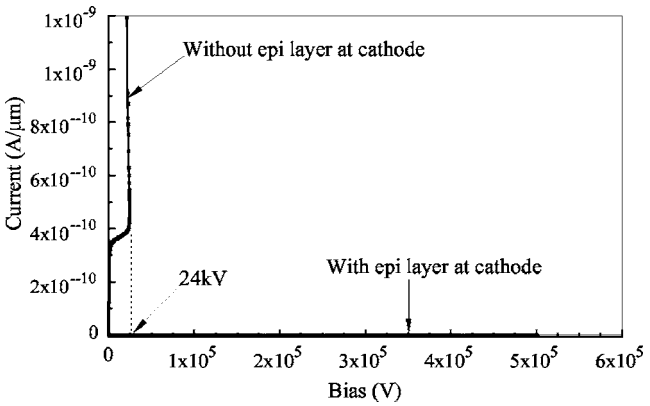

FIG. 4. Improvement in the hold off voltage due to p^+ layer at cathode (reproduced from Ref. 18).

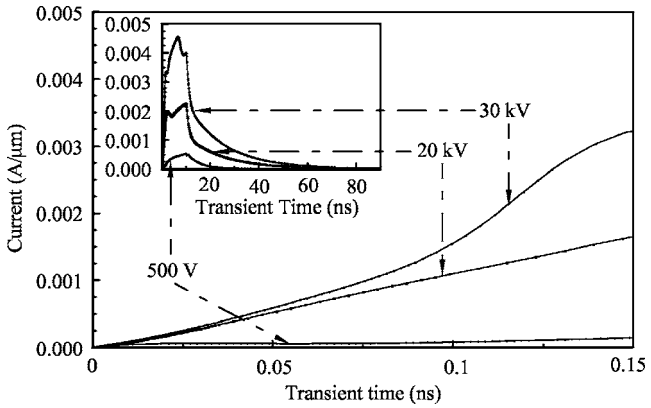

FIG. 6. Simulated rise time of the switch at higher bias conditions [experimental data at 500 V shown here matched with simulations, Fig 3(b)].

semiconductor field-effect transistors (MOSFETs) as a result of charge accumulation near the gate, following a single charge particle incident at this region.[18] Thus mechanisms that would lower the fields in the bulk material or limit the number of primary electrons to reach the anode could result in a switch operation at higher bias. Such a mechanism for high field operations with a n^+ layer at the cathode has been suggested earlier for DDSA-type GaAs PCSS.[19] For the SiC PCSS, however, simulations suggest that a p^+ region next to the cathode in the SDDA material would also allow us for higher bias operation, much beyond the current value of 18 kV (0.45 MV/cm) (Fig. 4, reported earlier[8] and is repeated here for convenience). The physical mechanism for the high bias operations in the SDDA SiC PCSS is different from that of a DDSA GaAs material. In case of the SiC PCSS, the interactions of the *p*-region and *n*-type bulk result in electron diffusion towards the p^+ region. The presence of the positively charged ionized donor N_{di}^+ in the bulk opposes the anode field, which results in a substantial lowering of the bulk field, as shown in Fig. 5. Impact ionization therefore is reduced substantially and as a result it is possible to increase the bias across the device without premature breakdown. Note that lowering the electric field inside the switch with the help of the p^+ layer allows the switch to be used more effectively as a linear switch (all the nonlinear effects minimized) minimizing surface flashover, filamentary conduction, premature breakdown, etc.[5]

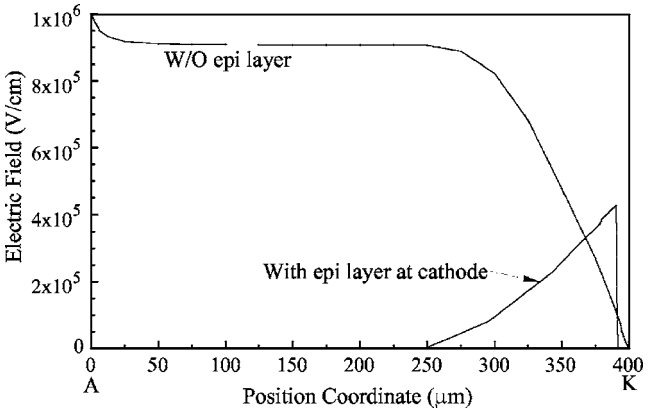

FIG. 5. Plot of electric field across the PCSS from anode to cathode with and without p^+ layer at the cathode.

The minimum thickness of the p^+ region next to the cathode for the SiC PCSS is also much less than the n^+ region for the DDSA GaAs switch. For a DDSA GaAs PCSS, it was reported that a minimum thickness of 20 μm of n^+ layer at cathode is required to achieve improvement in the hold off voltage.[19] This is primarily due to the fact that the material must be at least a diffusion length in thickness ($L_n = 10-15$ μm), to be effective.[20] For SiC the diffusion lengths are much smaller.[21] Simulations show that an improvement in the hold off voltage is possible for a few micron thick p^+ epilayers.

The simulated response of the PCSS to high field illumination is shown in Fig. 6. Here the illumination wavelength (532 nm, 2.33 eV) is less than the material band gap of 3.02 eV, since the switch is designed to operate in the extrinsic mode. The response to illumination, specifically the rise time, depends on the bias across the device (inset of Fig. 6) and the rise time of the switch improves with increasing bias. This is primarily because at higher bias, the effective depletion of the bulk increases. Thus the drift component of the currents increases leading to improved risetimes, as Fig. 6 shows. For the 500 V bias, the photocurrent followed the optical pulse with about 8 ns required to reach the peak value for both the experimental and simulated plots. For simulations at 20 and 30 kV, the peak show peak values at 6 and 2 ns, respectively, because higher contributions from the drift current component. Saturation is achieved at higher bias and the rise time is then limited mainly by the external circuit. A shorter lifetime translates to improved energy transmission to the load, and is an important design requirement, specifically for PCSS used in circuitry for generating high power microwaves (HPMs).

IV. CONCLUSION

The characteristics of a 6*H*-SiC PCSS are studied in order to investigate methods of improving the behavior in high field applications as in circuitry for generating ultrawideband high power microwaves, pulse generation, etc. The dielectric strength failure or breakdown of the switch at lower fields than the bulk dielectric strength of SiC has been analyzed through simulation. The physics of the breakdown mechanism appears to be due to injection of electrons at the

cathode, which result in nonuniform charge distribution and thus nonuniform electric field across the switch due to electron avalanche. A proposed method for reducing the nonuniform electric field distribution in the shallow donor, deep acceptor-type compensated material that is incorporating a p^+ layer next to the cathode, results in homogenous bulk field. Thus, the proposed method reduces the peak magnitude of the electric field in the switch which results in a higher operating voltage. As a result the current experimental hold off voltage of the switch would be increased by a factor of 5 (2.5 MV/cm). The minimum thickness of the p^+ layer necessary to avoid breakdown at voltages below the bulk dielectric strength is about a diffusion length. Additionally, the p^+ layer at the cathode also results in improved rise time for the PCSS when compared to the one without a p^+ layer.

ACKNOWLEDGMENTS

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[1]W. C. Nunnally, IEEE Trans. Electron Devices **37**, 2439 (1990).
[2]J. S. H. Schoenberg, J. W. Burger, J. S. Tyo, M. D. Abdalla, M. C. Skipper, and W. R. Buchwald, IEEE Trans. Plasma Sci. **25**, 327 (1997).
[3]G. M. Loubriel, M. W. O'Malley, and F. J. Zutavern, Pulse Power Conference, Digest of Technical Papers, PPC 1987, 6th IEEE International, edited by P. J. Truchi and B. H. Bernstein, Arlington, VA, 1987 (IEEE, New York, 1987), pp. 577–580.
[4]M. E. Levinshtein, S. L. Rumyantsev, and M. S. Shur, *Properties of Advanced Semiconductor Materials* (Wiley, New York, 2001).
[5]P. G. Neudeck, Institute of Physics Conference Series 141: Compound Semiconductors, presented at the 21st International Symposium of Compound Semiconductors, San Diego, CA (IOP, Bristol, 1994), pp. 1–6.
[6]S. Dogan *et al.*, Appl. Phys. Lett. **82**, 3107 (2003).
[7]W. Nunnally and M. Mazzola, Pulse Power Conference, Digest of Technical Papers, PPC 2003, 14th IEEE International (IEEE, New York, 2003).
[8]K. S. Kelkar, N. E. Islam, C. M. Fessler, and W. C. Nunnally, J. Appl. Phys. **98**, 093102 (2005).
[9]V. Lauer, A. Soufi, K. Chourou, M. Anikin, B. Clerjaud, and C. Naud, Mater. Sci. Eng., B **B61**, 248 (1999).
[10]J. R. Jenny, M. Skowronski, W. C. Mitchel, H. M. Hobgood, R. C. Glass, G. Augustine, and R. H. Hopkins, J. Appl. Phys. **78**, 3839 (1995).
[11]C. Mittchel, R. Perrin, J. Goldstein, A. Saxler, M. Roth, S. R. Smith, J. S. Solomon, and A. O. Evwaraye, J. Appl. Phys. **86**, 5040 (1999).
[12]M. Syväjärvi, R. Yakimova, A.-L. Hylén, and E. Janzén, J. Phys.: Condens. Matter **11**, 10041 (1999).
[13]S. M. Sze, *Physics of Semiconductor Devices* (Wiley-Interscience, New York, 1969).
[14]*Atlas User's Manual*, 7th ed. (Silvaco International, Santa Clara, CA, 2000), www.silvaco. com.
[15]R. Weingärtner, P. J. Wellmann, M. Bickermann, D. Hofmann, T. L. Straubinger, and A. Winnacker, Appl. Phys. Lett. **80**, 71 (2002).
[16]T. V. Blank, Yu. A. Goldberg, E. V. Kalinina, O. V. Konstantinov, A. O. Konstantinov, and A. Hallén, Semicond. Sci. Technol. **20**, 710 (2005).
[17]H. X. Yuan and A. G. U. Perera, J. Appl. Phys. **79**, □ (1996).
[18]J. R. Brews, M. Allenspach, R. D. Schrimpf, K. F. Galloway, J. L. Titus, and C. F. Wheatley, IEEE Trans. Nucl. Sci. **40**, 1959 (1993).
[19]N. E. Islam, E. Schamiloglu, J. S. H. Schoenberg, and R. P. Joshi, IEEE Trans. Plasma Sci. **28**, 1512 (2000).
[20]D. Ritter, K. Weiser, and E. Zeldov, J. Appl. Phys. **62** (1987).
[21]M. Tabib-Azar, S. M. Hubbard, C. M. Schnabel, and S. Bailey, J. Appl. Phys. **84** (1998).